REMARKS

Claims 29-39 and 41-49are all the claims presently pending in the application. Claim 40 has been canceled. Claims 29-33, 35-36 and 41-45 have been amended to more particularly define the invention. Claims 46-49 have been added to claim additional features of the invention. Attached hereto is a marked-up version of the changes made to the specification and claims by the current Amendment.

It is noted that the claim amendments are made only for more particularly pointing out the invention, and <u>not</u> for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability.

Claims 29-39 and 41-45 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Witek et al. (U.S. Pat. 6,146,970). Claims 29-39 and 41-45 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Chen et al. (U.S. Pat. 5,767,549). Claims 29-39 and 41-45 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Tsuchiaki (U.S. Pat. 6,051,509).

These rejections are respectfully traversed in view of the following discussion.

I. THE CLAIMED INVENTION

The claimed invention is directed to a semiconductor device which includes a bulk silicon region comprising single crystal silicon and a silicon-on-insulator (SOI) region. Further, the SOI region includes <u>an insulator layer which is formed beneath an upper portion of the single crystal silicon and has at least one lateral end portion adjacent to a lower portion of the single crystal silicon</u>, and at least one isolation oxide formed in the upper portion of the single crystal silicon so as to form at least one island of the single crystal silicon on an upper surface of the insulator layer.

Conventional substrates are formed of <u>either</u> SOI regions or bulk silicon regions. However, it is desirable to include different devices on the substrate, some of which are preferably formed on bulk silicon, and some of which are preferably formed on SOI. Therefore, if both types of these devices are formed on one substrate (e.g., bulk silicon), some performance sacrificed with respect to the type of device preferring the other substrate (e.g., SOI).

The claimed device, on the other hand, has a bulk silicon region and an SOI region. Specifically, the SOI region includes an insulator layer which is formed beneath an upper portion of the single crystal silicon and has at least one lateral end portion adjacent to a lower portion of the single crystal silicon, and at least one isolation oxide formed in the upper portion of the single crystal silicon so as to form at least one island of the single crystal silicon on an upper surface of the insulator layer. Therefore, unlike conventional devices, the claimed device can efficiently accommodate devices which are preferably formed on SOI and devices which are preferably formed on bulk silicon.

II. THE PRIOR ART REFERENCES

A. The Witek Reference

The Examiner alleges that Witek discloses the claimed method. Applicant submits, however, that there are elements of the claimed method which are neither taught nor suggested by Witek.

Witek discloses a method of forming a capped shallow trench isolation which includes forming a trench region within a substrate, depositing a first trench fill material within the trench region after forming a first liner region, removing a portion of the first trench fill material to form a first trench plug region within the trench region, removing a portion of the first trench fill material to form a first trench plug region within the trench region, removing a portion of the first liner region to expose a portion of the substrate, depositing a second trench fill material overlying the first trench plug region, and removing a portion of the second trench fill material to form a second trench plug region (Witek at col. 11, lines 25-49).

However, Witek does not teach or suggest an SOI region which includes "an insulator layer which is formed beneath an upper portion of said single crystal silicon and has at least one lateral end portion adjacent to a lower portion of said single crystal silicon" nor "at least one isolation oxide formed in said upper portion of said single crystal silicon so as to form at least one island of said single crystal silicon on an upper surface of said insulator layer" all of which is recited in claim 29 and similarly recited in claims 41 and 45.

As explained in the Application, conventional semiconductor devices are often

formed on one of either SOI substrate or bulk silicon substrate (Application at page 2, lines 2-10). However, some devices are not easily formed on SOI substrates. Further, some devices are preferably formed on bulk silicon and some devices are preferably formed on SOI substrate (Application at page 2, lines 14-20). Therefore, if both types of these devices are formed on one substrate (e.g., bulk silicon), some performance sacrificed with respect to the type of device preferring the other substrate (e.g., SOI).

The claimed device, on the other hand, has an SOI region which includes <u>an insulator layer which is formed beneath an upper portion of the single crystal silicon and has at least one lateral end portion adjacent to a lower portion of the single crystal silicon</u> (Application at Figure 1D; page 7, lines 12-21). Further, the <u>upper portion of the single crystal silicon may be formed over said insulator layer by depositing</u> amorphous silicon <u>on the insulator layer and the lower portion of the single crystal silicon, and horizontally growing the single crystal silicon over the insulator layer using the lower portion of the single crystal silicon as a crystal growth seed</u> (Application at page 7, lines 19-21). For instance, the Application explains that the insulator layer may have a thickness <u>in a range of 1000Å and 5000Å</u> (Application at page 7, lines 15-16).

The SOI region further includes <u>at least one isolation oxide formed in the upper portion of the single crystal silicon so as to form at least one island of the single crystal silicon on an upper surface of the insulator layer</u> (Application at Figure 1D). More specifically, the isolation oxides may be formed in defective areas of the single crystal silicon (Application at Page 7, line 22-page 8, line 11).

Therefore, unlike conventional devices, the claimed invention can efficiently accommodate both devices preferably formed on SOI (e.g., high speed or noise-sensitive circuits, such as DRAM arrays) as well as devices preferably formed on bulk silicon (e.g., temperature-sensitive circuits such as logic devices). (Application at Figure 2G; page 7, line 7-page 8, line 11).

Clearly, Witek does not teach or suggest these novel features. Indeed, <u>Witek does not even show a device having both a bulk silicon region and an SOI region</u>. Certainly, Witek can not teach or suggest an SOI region having an insulator layer and isolation oxides as in the claimed device.

For instance, the Examiner relies on Figure 14 of Witek to support his argument. However, Figure 14 merely shows active regions 220, 230, 240. For instance, region 240 includes substrate 202, source and drain regions 256, 258, trench liner material 212, trench fill material 216c, silicon nitride cap 218b, silicon dioxide gate 250 and polysilicon gate electrode 272 (Witek at Figure 14). In other words, nowhere in Figure 14 does Witek show the novel features of the claimed device, specifically, an insulator layer and isolation oxides formed on the insulator layer.

Moreover, Applicant reiterates that the Examiner is improperly relying on the statement in Witek that "[t]ypical semiconductor substrates 202 are either silicon wafers ... silicon on insulator (SOI) substrates ... or the like (Witek at col. 6, lines 7-11). Clearly, this passage says nothing about forming a substrate having both a silicon and an SOI region. Indeed, Applicant notes that the passage includes the words "either" and "or", as to say that the semiconductor substrate 202 in the Witek structure is either formed of a silicon substrate or an SOI substrate. In other words, referring to Figure 14, the semiconductor substrate 202 may be either silicon or SOI, but is certainly not both.

Therefore, Applicant submits that Witek does not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

B. The Chen Reference

The Examiner alleges that Chen discloses the claimed method. Applicant submits, however, that there are elements of the claimed method which are neither taught nor suggested by Chen.

Chen discloses a silicon-on-insulator (SOI) CMOS structure which is intended to overcome floating gate problems caused by charge accumulation below the channel of metal oxide semiconductor field effect transistors (MOSFETs). The Chen device includes a substrate, a layer of insulator, a layer of silicon having raised mesas and thin regions therebetween to provide ohmic conduction between mesas, electronic devices on the mesas, and interconnection wiring (Chen at Abstract).

However, like Witek, Chen does not teach or suggest an SOI region which includes

"an insulator layer which is formed beneath an upper portion of said single crystal silicon and has at least one lateral end portion adjacent to a lower portion of said single crystal silicon" nor "at least one isolation oxide formed in said upper portion of said single crystal silicon so as to form at least one island of said single crystal silicon on an upper surface of said insulator layer" all of which is recited in claim 29 and similarly recited in claims 41 and 45.

As explained above, the claimed device, unlike conventional devices, has an SOI region which includes an insulator layer which is formed beneath an upper portion of the single crystal silicon and has at least one lateral end portion adjacent to a lower portion of the single crystal silicon (Application at Figure 1D; page 7, lines 12-21). Further, the upper portion of the single crystal silicon may be formed over said insulator layer by depositing amorphous silicon on the insulator layer and the lower portion of the single crystal silicon, and horizontally growing the single crystal silicon over the insulator layer using the lower portion of the single crystal silicon as a crystal growth seed (Application at page 7, lines 19-21). For instance, the Application explains that the insulator layer may have a thickness in a range of 1000Å and 5000Å (Application at page 7, lines 15-16).

The SOI region further includes at least one isolation oxide formed in the upper portion of the single crystal silicon so as to form at least one island of the single crystal silicon on an upper surface of the insulator layer (Application at Figure 1D). More specifically, the isolation oxides may be formed in defective areas of the single crystal silicon (Application at Page 7, line 22-page 8, line 11).

Therefore, unlike conventional devices, the claimed invention can efficiently accommodate both devices preferably formed on SOI (e.g., high speed or noise-sensitive circuits, such as DRAM arrays) as well as devices preferably formed on bulk silicon (e.g., temperature-sensitive circuits such as logic devices). (Application at Figure 2G; page 7, line 7-page 8, line 11).

Clearly, Chen does not teach or suggest these novel features. Indeed, Applicant directs the Examiner's attention to the title of the Chen device which reads "SOI CMOS Structure". In other words, Chen merely discloses an SOI substrate, not a combined bulk silicon and SOI substrate.

Further, the Examiner refers to Figure 1 in Chen and asserts that Chen discloses "an

SOI region 14 comprising a single crystal silicon ... and islands of crystal silicon form STI's 38 formed at predetermined locations to remove defects on the SOI region". However, Applicant notes that nowhere does Figure 1 show an SOI region having a insulator layer having at least one lateral end portion adjacent to a lower portion of said single crystal silicon as in the claimed device. Instead, the dielectric 14 in Figure 1 of Chen covers the entire substrate12. Therefore, Chen cannot teach or suggest the novel hybrid substrate of the claimed device.

Further, Applicant notes that the Chen device may include STI oxides 38 (Chen at Figure 1). However, these STI oxides 38 are not formed on an insulator layer as in the claimed device. Therefore, these islands cannot be equated with the isolation oxides in the claimed device.

Further, Chen clearly teaches an insulating layer 14 that runs the length of the substrate and therefore, a device could not access bulk silicon in the Chen device.

In addition, as shown in the Application at Figure 1D, the resulting structure of the claimed invention allows devices formed in the SOI region to be completely isolated from other devices. Note, for instance that a device can be formed on one of the silicon islands between the oxides 104 and be completely isolated from a device on another silicon island. This is completely different, for example, than the Chen device in which the isolation oxide 38 does not completely isolate the left and right device (Chen at Figure 1).

Therefore, Applicant submits that Chen does not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

C. The Tsuchiaki Reference

The Examiner alleges that Tsuchuiaki discloses the claimed method. Applicant submits, however, that there are elements of the claimed method which are neither taught nor suggested by Tsuchiaki.

Tsuchiaki discloses a method of forming an integrated circuit device which includes forming a first carbon-containing semiconductor layer in a first region on a surface of a semiconductor substrate, forming a second carbon-containing semiconductor layer in a

second region on the surface, and forming first and second gate-insulation layers in the first and second carbon-containing semiconductor layer, each gate-insulation layer having a film thickness dependent on the carbon content in the corresponding carbon-containing semiconductor layer (Tsuchiaki at col. 21, line 64-col. 65, line 10).

However, like Witek and Chen, Tsuchiaki does not teach or suggest an SOI region which includes "an insulator layer which is formed beneath an upper portion of said single crystal silicon and has at least one lateral end portion adjacent to a lower portion of said single crystal silicon" nor "at least one isolation oxide formed in said upper portion of said single crystal silicon so as to form at least one island of said single crystal silicon on an upper surface of said insulator layer" all of which is recited in claim 29 and similarly recited in claims 41 and 45.

As explained above, the claimed device, unlike conventional devices, has an SOI region which includes an insulator layer which is formed beneath an upper portion of the single crystal silicon and has at least one lateral end portion adjacent to a lower portion of the single crystal silicon (Application at Figure 1D; page 7, lines 12-21). Further, the upper portion of the single crystal silicon may be formed over said insulator layer by depositing amorphous silicon on the insulator layer and the lower portion of the single crystal silicon, and horizontally growing the single crystal silicon over the insulator layer using the lower portion of the single crystal silicon as a crystal growth seed (Application at page 7, lines 19-21). For instance, the Application explains that the insulator layer may have a thickness in a range of 1000Å and 5000Å (Application at page 7, lines 15-16).

The SOI region further includes at least one isolation oxide formed in the upper portion of the single crystal silicon so as to form at least one island of the single crystal silicon on an upper surface of the insulator layer (Application at Figure 1D). More specifically, the isolation oxides may be formed in defective areas of the single crystal silicon (Application at Page 7, line 22-page 8, line 11).

Therefore, unlike conventional devices, the claimed invention can efficiently accommodate both devices preferably formed on SOI (e.g., high speed or noise-sensitive circuits, such as DRAM arrays) as well as devices preferably formed on bulk silicon (e.g., temperature-sensitive circuits such as logic devices). (Application at Figure 2G; page 7, line

7-page 8, line 11).

Clearly, Tsuchiaki does not teach or suggest these novel features. The Examiner refers to Figure 6(b) of Tsuchiaki as showing the claimed device. However, Figure 6(b) merely shows a silicon substrate 200, STI layer 201 channel dopant region 202, and silicon dioxide layer 206. Clearly, none of these features can be equated with the insulator layer of the claimed device.

Further, the STI layers 201 clearly cannot be equated with the isolation oxides of the claimed device because the STI layers 201 are not formed on an insulator layer. Indeed, Applicant notes that the STI layer 201 is apparently formed on the silicon substrate 200. Moreover, the STI layers 201 are clearly not formed so as to form islands of single crystal silicon on an insulator layer. Figure 6(b) clearly does not teach or suggest the isolation oxides as in the claimed device.

Further, assuming that the Examiner equates the substrate 200 as the SOI region, Tsuchiaki merely states that the substrate 200 may be <u>either</u> bulk silicon <u>or</u> SOI (Tsuchiaki at col. 21, lines 10-21). Nowhere does Tsuchiaki suggest a structure which includes both a SOI substrate and a bulk silicon substrate.

Therefore, Applicant submits that Tsuchiaki, like Witek and Chen, does not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

IV. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 29-39 and 41-49, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a <u>telephonic or personal interview</u>.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 50-0510.

Respectfully Submitted,

Date: 3/4/02

Phillip E. Miller
Reg. No. 46,060

McGinn & Gibb, PLLC
8321 Old Courthouse Road, Suite 200
Vienna, VA 22182-3817
(703) 761-4100
Customer No. 21254

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claim 40 has been canceled.
Claims 46-49 have been added.
The claims were amended as follows:

29. (Amended) A semiconductor device comprising:

a bulk silicon region comprising single crystal silicon; and

a silicon-on-insulator (SOI) region comprising:

an insulator layer which is formed beneath an upper portion of said single crystal silicon and has at least one lateral end portion adjacent to a lower portion of said single crystal silicon; and

at least one isolation oxide formed in said upper portion of said single crystal silicon so as to form at least one island of said single crystal silicon on an upper surface of said insulator layer

[a crystallized silicon layer formed by annealing amorphous silicon and having isolation trenches formed therein so as to remove defective regions, and

isolation oxides formed in said isolation trenches].

30. (Amended) The semiconductor device according to claim 29, wherein said at least one island of single crystal [islands of crystallized] silicon comprises a plurality of islands and said at least one isolation oxide comprises a plurality of isolation oxides, and each of said islands are interspaced between said isolation oxides to form a shallow trench isolation (STI) structure.

31. (Amended) The semiconductor device according to claim 30, wherein said [SOI region further comprises: an] insulator layer has a thickness in a range of 1000Å and 5000Å [underneath said STI structure].

32. (Amended) The semiconductor device according to claim 29, wherein said upper portion of said single crystal silicon is formed over said insulator layer by depositing

amorphous silicon on said insulator layer and said lower portion of said single crystal silicon, and horizontally growing said single crystal silicon over said insulator layer using said lower portion of said single crystal silicon as a crystal growth seed [is crystallized using an exposed portion of silicon as a seed].

33. (Amended) The semiconductor device according to claim 32 [30], wherein said isolation oxides are formed in defective portions of said single crystal silicon [between adjacent devices on said semiconductor device].

35. (Amended) The semiconductor device according to claim 29, wherein an upper surface of said isolation oxides and said single crystal [crystallized] silicon [layer] are planarized.

36. (Amended) The semiconductor device according to claim 29, wherein said single crystal [crystallized] silicon [layer] over said insulator layer has a same crystal orientation and structure as said single crystal silicon in said bulk silicon region [which follows that of an underlying substrate].

41. (Amended) A hybrid bulk silicon and silicon-on-insulator (SOI) substrate, comprising:

an insulator layer which is formed beneath an upper portion of single crystal silicon and has at least one lateral end portion adjacent a lower portion of said single crystal silicon; and

a plurality of isolation oxides formed in said upper portion of said single crystal silicon so as to form at least one island of said single crystal silicon on an upper surface of said insulator layer

[a crystallized silicon layer formed by annealing amorphous silicon and having isolation trenches formed therein so as to remove defective regions; and

isolation oxides formed in said isolation trenches].

42. (Amended) The hybrid substrate according to claim 41, wherein said insulator layer is formed only in [further comprising: bulk silicon region; and] an SOI region of said substrate and not in a bulk silicon region of said substrate [, wherein said crystallized silicon layer and said isolation oxides are formed in said SOI region].

43. (Amended) The hybrid substrate according to claim 42, wherein said substrate is part of a semiconductor device comprising a logic device [is] formed in said silicon-on-insulator (SOI) region.

44. (Amended) The hybrid substrate according to claim 42, wherein said substrate is part of a semiconductor device comprising a memory device [is] formed in said bulk silicon region.

45. (Amended) A semiconductor device comprising:

a bulk semiconductor region comprising semiconductor substrate; and

a semiconductor-on-insulator region comprising:

an insulator layer which is formed beneath an upper portion of said semiconductor substrate and has at least one lateral end portion adjacent to a lower portion of said semiconductor substrate; and

at least one isolation oxide formed in said upper portion of said semiconductor substrate so as to form at least one island of said semiconductor substrate on an upper surface of said insulator layer

[a crystallized semiconductor layer formed by annealing amorphous semiconductor and having isolation trenches formed therein so as to remove defective regions, and

isolation oxides formed in said isolation trenches].